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System DFT Guidelines

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Design for Test Guidelines For System Level Testing and In-System Configuration

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Preface:

Boundary-Scan Technology For PCB Testing and In-System Configuration

Why boundary-scan?

Throughout the electronics industry, manufacturers are turning to the latest device technologies, such as ball-grid arrays (BGAs), chip-scale packages, and other small outlines, to provide the functionality and miniaturization they need. However, the new packages are increasing the difficulty of accessing printed circuit boards for In-Circuit Testing (ICT) and in-system device programming. These difficult access problems have been addressed by the industry through adoption of the IEEE 1149.1 boundary-scan standard, allowing pin-level access - independent of the device packaging technology - to even the most crowded assemblies. Nowadays almost all popular complex ICs are supporting IEEE Std 1149.1 test features. Boundary-scan has been industry-wide accepted as means to access electronic assemblies (multi-chip modules, printed circuit boards, (sub)-systems), not only for testing, but also for in-system programming. Once boundary-scan has been implemented on printed circuit board level (with or without the help of our 'Board DFT Guidelines' booklet), its application could also be extended to system level. The guidelines described in this booklet help the designer to implement system level design for test (DFT).

Benefits of boundary-scan at system level

The benefits of implementing system level test access by extending boundary-scan to the backplane (creating a unified test strategy for board and system level based on the IEEE Std. 1149.1 architecture) can be enormous. We will just describe the possibilities and opportunities which you can translate these to your own situation.

It provides the user a low cost solution for system-wide communication with one single point of access for testing of printed circuit boards and their interconnections (e.g. backplanes), for in-system programming of flash memories, for in-system (re-) configuration of PLDs using IEEE 1532 and for maintenance.

It supports board and system level BIST strategies and allows the re-use of test vectors for testing at the device, board and system level test as well for using an embedded controller in support of a remote boundary-scan test capability. In the conventional way each stage in the product life cycle had its own particular test method: trial and error at rack and stack systems during development or engineering for prototype debugging, in-circuit testing for Printed Circuit Boards followed by functional testing at PCB or sub-assembly level during manufacturing, system operation as final system testing during factory clearance or installation test at the customer's site and finally for service and maintenance pragmatic, low cost tools. All these different test methods need their specific test preparation engineering efforts to generate a test program. That means for one and the same design the test engineering effort is increased three fold! With a unified test strategy based on boundary-scan you will do it once and the test programs can be used and re-used throughout the product life cycle.

Besides the savings of test (engineering) effort there are large benefits at the use of the systems in the field. The system level test access architecture provides a comprehensive diagnostic test capability - either locally or remotely - without the overhead of board and system level test software. It supports remote system upgrades or field reconfiguration in case certain components are failing. Last but not least thanks to more accurate pin level diagnostics you have much better control over your field spare inventory.

Application examples are an embedded tester that can simplify military system logistics by eliminating the need for a dedicated field test system. Or, an embedded test function in a telecommunication system that allows the system administrator to determine the exact cause of a system malfunction. The request for field support could include a description of the field replaceable unit. When the engineer arrives on site the needed part will arrive too. Vendors who provide embedded test systems can exceed their customer's expectations whether they supply commercial or military systems!

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1 Introduction

So, at last you've managed to grab a five minute break to take a closer look at what you can do with that puzzling interface people have been talking about - the JTAG port. If you've studied it in detail you will have realised that by using the completely autonomous JTAG port you can access all the pins (except analogue, power and grounds) of a JTAG compliant part with the core logical function effectively disconnected or suspended. This means that via a minimal 4 wire bus you can use test patterns (vectors) to toggle signals at output or I/O pins and monitor inputs at sense or I/O pins to establish whether or not interconnects (nets) are as per your design.

If you are a design engineer reading this then you will already have acknowledged the role you must play in DFT (Design for Test). If however you are a test or production engineer it is vital that you establish contact with designers at the earliest planning stages of a new design and gain their co-operation to implement some of the ideas mentioned below. In either instance it is clearly advantageous to have regular meetings on a products test strategy (for prototype debug, production and field service) as soon as product concepts are known.

The scope of this document is to present a number of Design-for-Test guidelines that can be used for reference in support of implementing system level boundary-scan architecture within PCB designs. So that this architecture can be utilised effectively in performing board level manufacturing structural testing and the in-system configuration of cPLD, FPGA's and flash memory devices within a system level environment.

This document also describes how this architecture can be further utilised to provide an integrated dynamic test capability at both system level test and in a field diagnostic environment.

2 Considerations for Implementing System Level Boundary-Scan

2.1 Architectural Decisions

2.1.1 Consider all Test Scenarios

In order to be able to implement a system level boundary-scan test strategy it is imperative that all possible usage scenarios are considered at the design conceptual stage i.e.

- Will system access only be required for manufacturing testing either at the functional or system level test stages?
- Is it envisaged that this test capability will be utilised within a field environment?
- Will it be a requirement to be able to utilise this test capability remotely i.e. does the control for executing boundary test vectors need to be embedded?

These considerations will be discussed in the following paragraphs with some guidelines on how to implement hierarchical boundary-scan architecture.

2.1.2 Multidrop Environment - External Controller Test Vector Delivery

Figure.1 depicts a backplane multidrop environment where each board is located within a backplane slot and each slot has its own unique address. Interface to the boards within the backplane is via a boundary-scan bus comprising of TCK, TMS, TDI, TDO, TRST and the AutoWrite signal to enable optimisation of flash programming operations.

This bus can be accessed via an external boundary-scan controller by interfacing to the backplane connector so that communication to individual cards within the backplane can be accomplished by broadcasting the relevant slot address via TDI. The card residing in that slot will wake-up and allow access to selected local scan chains under the control of the system access protocol.

This type of architecture will allow tests that have previously been developed for stand alone board level manufacture structural testing and in-system configuration, to be re-used within a system level environment to enhance the diagnostic capability and in-system configurability.

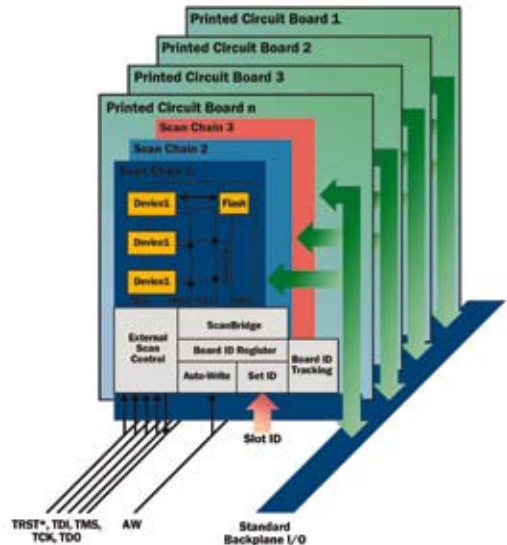


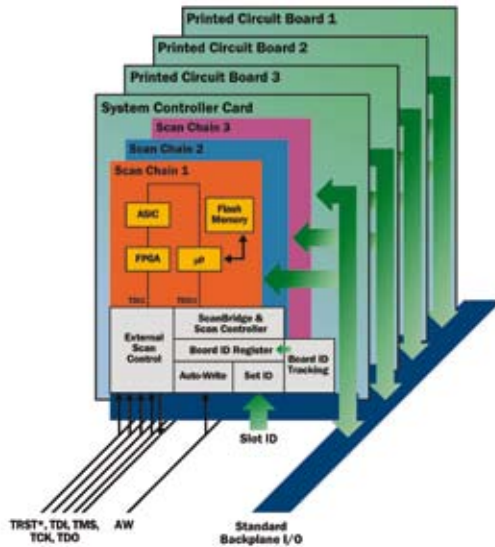
Figure. 1 - Multidrop Configuration (External Test Controller)

2.1.3 Multidrop Environment - Embedded Controller Test Vector Delivery

Alternatively it may be a requirement to be able to utilise this test capability within a field application environment for remote diagnostics or downloading a new version of flash memory code or to update

cPLD and FPGA objects. This can be accomplished by embedding the test vector delivery capability within a system master controller card as shown in Figure.2 below.

Figure. 2 - Multidrop Configuration (Embedded Test Controller)



The system level configuration depicted in figure.2 is similar to that shown in figure.1 except that the JTAG controller is now embedded within the System Controller card and the test vectors that were previously stored on the hard disk of the system test platform or on a laptop for field support, are now stored within flash memory on the System Controller card.

In this configuration the System Controller card will have complete control of test vector delivery and will execute the system access protocol necessary to communicate with all boards within the backplane, either separately or as a pre-defined multi-cast group.

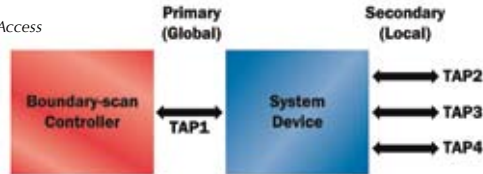
Communication with the embedded controller will be under the control of System Controller card processor which will be performing read/write accesses between the flash memory and the scan controller device.

2.2 System Level Access

2.2.1 System Device Functionality

System access between the system level JTAG bus and individual local scan chains on individual boards within system level environment necessitates the implementation of at least one system access device on each card residing within each of the backplane slots similar to that shown in Figure.3.

Figure. 3 - System Level Access



2.2.2 Local Scan Port Configuration

A system level device will provide access via a single primary TAP port interface which will be hooked up to the JTAG backplane bus, to a minimum of 3 local scan ports (there are a variety of devices that will support more than 3 scan ports), each connected to its respective scan chain.

By addressing the system interface device and communicating with its internal state machine using a proprietary protocol, it is possible to connect the primary interface port to each of the local scan chains in isolation or by any combination of scan chains daisy chained together i.e. TAP2 and TAP3, TAP3 and TAP4, TAP2 and TAP4 or in one chain consisting of TAP2, TAP3 and TAP4.

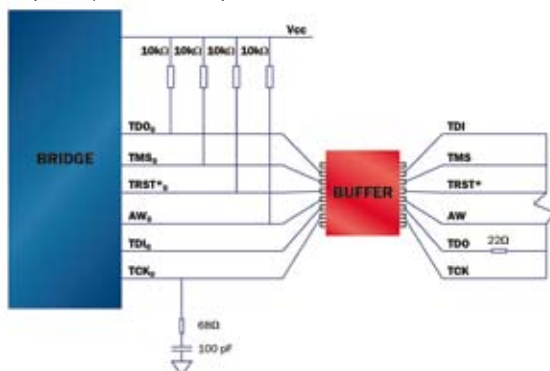
This is extremely versatile as it allows a single chain combination for executing board level interconnect testing or single TAP access for either optimised flash programming, in-system configuration, or localised cluster testing.

2.2.3 Local Scan Port Terminations

For all applications the LSP signals from the bridge devices should be correctly terminated as previously detailed in sub-paragraph.2.2.1. This is to ensure that once the bridge device is deselected, the LSP signal lines are held in a known state.

The buffer device in Figure.4 below is not only utilised for fan out of TCK and TMS signals as previously detailed in sub-paragraph.2.3.2., but also for providing adequate drive strength for the LSP signals, particularly where the bridge functionality is embedded (IP core) within a cPLD device as the standard drive capability from the IO pins will be insufficient.

Figure. 4 - Local Scan Port Terminations



2.3 System Level Access Devices

2.3.1 Device Types and Vendors

A variety of system level devices have been developed by a number of silicon manufacturers to support system level access, and the table depicted in Figure.5 endeavours to provide details of the type of device and the name of the relevant silicon vendor. However, it is not the intention within this document to describe the function of every device in absolute detail, but to indicate the plethora of devices available so that you can access the relevant web sites for more details.

Figure. 5 - Device Types and Vendors

Device	Name	Semi-house
JTS03 (IP Core or as device)	Gateway Device	Firecron Ltd
JTS06 (IP Core or as device)	Gateway Device	Firecron Ltd
SCANSTA111	ScanBridge	National Semiconductor
LSC BSCAN-1	Multiple Scan Port	Lattice Semiconductor
LSC BSCAN-2	Scan Path Linker	Lattice Semiconductor
SN54/74LVT8996	Addressable Scan Port	Texas Instruments
SN54/74ACT8997	Scan-Path Linker	Texas Instruments

Note: - Each of the devices detailed in figure.5 above come in a number of package styles and has their own individual merits and limitations. It is not the intention of this document to fully analyse the respective merits or limitations, but to describe a variety of system level chipset features so that designers and test engineers can determine what features they need to support their individual test and system architectural requirements.

2.4 System Level Device Features

2.4.1 How Many Local Scan Ports?

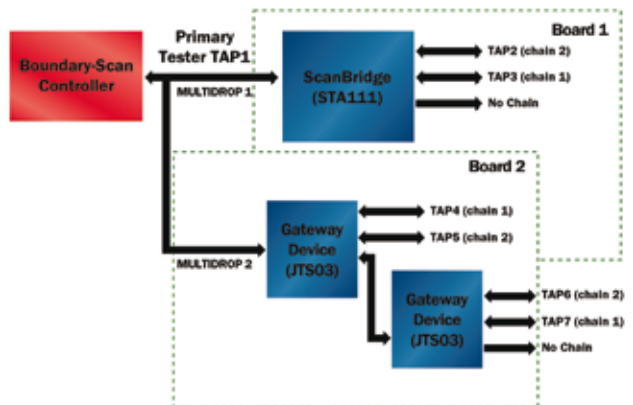
Depending on your board level architecture, you will need to consider how many local scan chains the system level interface device will support. The minimum is three; however, there are variants from Firecron Ltd and National Semiconductor that will support six and five local scan chains respectively.

2.4.2 Does the System Level Interface Device Support Multidrop Access

If your system level backplane design is going to implement a slot addressable multidrop architecture, you must ensure that the system level devices implemented within your board designs will support multidrop addressing as shown in Figure.6 below.

Figure. 6 - Multidrop Access

In the above example **Board 1** and **Board 2** are selected by broadcasting the multidrop 1 and multidrop 2 slot addresses respectively, and then selecting the relevant local scan chain (or chains) as required for executing the boundary-scan tests.



2.4.3 Does the Bridge Device Support Parking of the Local Scan Chains

In order to support board-to-board interconnect testing it is imperative that the bridge/gateway device is capable of supporting the PARKPAUSE instruction which will place all unparked local scan ports (LSP's) in one of the TAP controller pause states; either PAUSE-DR or PAUSE-IR. After shifting the appropriate test data into the boundary-scan registers of the respective boundary-scan devices and entering the PAUSE-DR TAP controller state. Multiple boards within a backplane environment can be sequenced through the Update and Capture states simultaneously, thus allowing interconnect tests to be conducted between boards within multiple slots.

2.4.4 Can Bridge Devices be Cascaded

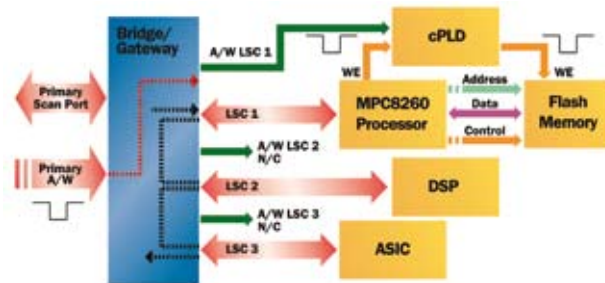
It may be necessary to cascade multiple bridge devices as shown for the Board 2 configuration in Figure.6. This is extremely useful where the selected bridge device will only support a maximum of 3 LSP's and access is required to more than 3 local scan chains. In this instance multiple bridge devices can be cascaded to access the requisite number of local scan chains, however, this will necessitate the placement of multiple devices on the board resulting in the overhead of more real estate. This problem can be resolved by cascading IP (Intellectual Property) cores into a single piece of silicon e.g. a cPLD. Some of the scan chipset silicon vendors will support this business model. The cascade feature is also a useful mechanism for connecting mother and daughter card combinations as described in sub-para. 2.5.1. to extend the boundary-scan test capability.

2.4.5 Does the Bridge Device Support AutoWrite™ Pass Through

As discussed in previous sections of this document it may be advantageous for the JTAG Technologies AutoWrite™ capability to be utilised to optimise access to flash memory clusters located in local scan chains connected to the bridge device. In this scenario there must be a mechanism for routing the AutoWrite™ signal connected to the primary side of the bridge device, through to selected LSP's on the secondary side of the bridge as shown in Figure.7. This capability is supported by some scan chipset providers, by either selecting the appropriate AW Register value or by direct pass through from the primary port to the secondary port of a selected LSP.

Note: - This capability is extremely important if the design group have made the provision to access flash memory WE signals via the outside world, thus enabling connection to the AutoWrite signal on the TAP pod. Only to find, that this capability cannot be utilised because the bridge device does not support the pass through feature.

Figure. 7 - AutoWrite™ Pass Through



2.4.6 Does the Bridge Device Support a Generic Pass-through Capability

It may be necessary to access cPLD or FPGA devices located in local scan chains directly using vendor specific JTAG programming or emulation tools. This will not be possible through a bridge/gateway device unless the selected bridge device supports a generic pass through capability.

*Note: - the JTAG programming and emulation tools from Xilinx, Altera and Lattice etc, do NOT support bridge/gateway protocol
 - JTAG Technologies tools DO support these protocols.*

This generic pass through feature is supported by some of the scan chipset providers by either selecting the appropriate binary combination on specific control lines in conjunction with a pass through enable signal as shown in Figure.8 or by shifting in the TRANSPARENTn instruction into the bridge device instruction register (where n is the selected LSP), and as the TAP controller goes through UPDATE-IR states, TRSTn will go high and TMS will go low. This will force targets connected to the LSPn ports to move to the RTI state.

As the bridge device state machine moves into the RTI state, all the LSP signals will follow the primary backplane signals, such that the bridge device becomes transparent.

Figure. 8 - Generic Pass Through



2.4.7 Does the Bridge Device Have the Capability for Reading-back Board ID and Revision

Depending upon the system level architecture it may be necessary that after establishing a board is present within a unique backplane slot location, to have the capability to read back the identity of the board located within that slot. This is particularly important within a system architecture where any board type can be located within any of the slots, which means that the identity of the board must be established before the appropriate test vectors can be broadcast to that slot address.

In this situation, it is not only the board identity that is important but also the revision/version of the board, which is often dependant on the version of the images programmed into cPLD's or the configuration objects stored in flash memory for configuring the FPGA devices.

This is particularly important when part of the test sequence is to verify that the cPLD / FPGA's have been configured correctly by reading back the device USERCODE value.

The board ID type and version control is user definable within a 16-bit Board ID register, which is hard-coded by connecting zero ohm resistors between the Board ID register pins and either Vcc or GND.

Figure. 9 - Board Identification Register



2.4.8 Additional Features

A number of the chipset devices have additional features, such as LSP_ACTIVE or BRIDGE_SELECT signal pins which are asserted once the bridge device is selected. This useful feature can be utilised to control a JTAG Enable pin (refer to sub-paragraph 2.1.2), to place dual function devices in boundary-scan mode or control some glue logic so that boundary-scan tests can be executed successfully.

2.5 Board-to-Board Testing

2.5.1 Mother / Daughter Card Interconnect Testing

A useful cascade application is the cascading of a mother/daughter card combination as shown in Figure.10 below, where the bridge device on the mother card is the primary bridge device and has direct access to the backplane JTAG bus, whereas the bridge device on the daughter card is the secondary bridge device within the cascaded configuration.

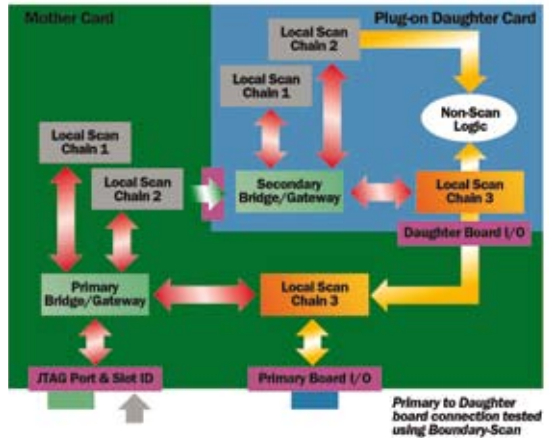


Figure. 10 - Mother/Daughter Card Interconnect Testing

2.5.2 Cascaded Bridge Device Configuration

The above cascaded configuration will allow the mother and daughter cards to be combined within a module assembly, so that the netlist for the two separate designs can be merged into a single netlist to describe the mother/daughter configuration inclusive of the mother-to-daughter card I/O mapping.

The bridge relationship between the mother and daughter cards can then be described in the connection (CON) file in the format detailed in Figure.11., where the secondary bridge device is shown cascaded to local scan port 2 of the primary bridge device.

Utilisation of the bridge devices in the above configuration, allow each card to be tested as separate entities during the manufacturing board test phase, and then to be combined as a module and tested a mother/daughter card combination at the system test phase.

Figure. 11 - CONnection File Configuration

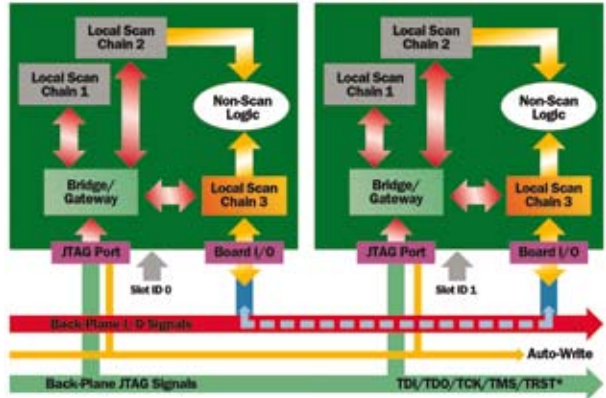
Scan Bridge Connection File

```
TESTER_CHANNEL TAP1
MULTIDROP1 (JTS03, 1, 0, TAP1, CASCADE1, TAP3)
CASCADE1 (STA111, 0, TAP4, TAP5, TAP6)
END_CHANNEL
```

2.5.3 Multidrop Interconnect Test Configuration

Boards located within a multidrop configuration will also support board-to-board interconnect testing as shown in Figure.12 below. In this configuration the backplane interconnect mapping can be defined within a separate netlist and merged with the netlist information from the cards located within each slot. The merged netlist can then be utilised to define the backplane connectivity, and identify the devices that need to be activated within each card to perform the board-to-board interconnect testing.

Figure. 12 - Multidrop Interconnect Testing



In the above example the interconnect test vectors are shifted into the individual cards via the bridge/gateway devices and the respective TAP controllers for the test execution devices placed in the PAUSE-DR state. Once the respective test stimulus is setup, the boards within this backplane configuration must move through the UPDATE-DR and CAPTURE-DR states simultaneously in order to capture the response data, before this data can be individually shifted out from each of the cards.

The simultaneous UPDATE and CAPTURE phases is achieved by utilising the broadcast and multicast addressing modes of the bridge devices.

2.5.3.1 Broadcast Addressing

The Broadcast address mode allows a JTAG controller to simultaneously select all bridge/gateway devices within a system environment. To avoid bus contention between scan-path output drivers on different cards, each bridge device's TDOB buffer is always tri-stated whilst in Broadcast mode.

2.5.3.2 Multicast Addressing

A technique for making the broadcast mechanism more selective is the Multi-cast addressing mode in which the bridge device multi-cast group register (MCGR) can be programmed to assign specific bridge devices to one of four multi-cast groups. When bridge devices in the WAIT-FOR-ADDRESS state are updated with a Multi-Cast address, all bridge devices whose MCGR match the broadcast multi-cast group address will be selected. As in Broadcast mode TDOB is always tri-stated.

3 Contact Information

For more information of JTAG Technologies:

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For more information of companies selling system level devices:

Firecron	http://www.firecron.com
Lattice Semiconductor	http://www.latticesemi.com
National Semiconductor	http://www.national.com/appinfo/scan/
Texas Instruments	http://www.ti.com/sc/docs/jtag/jtaghome.html

IEEE Standards:

- IEEE Std 1149.1-2001 - IEEE Standard Test Access Port and Boundary-Scan Architecture (Supersedes former issues IEEE 1149.1-1990 (Including 1149.1a-1993) and IEEE 1149.1b-1994 and errata)
- IEEE Std 1532-2001 - IEEE Standard for In-System Configuration of Programmable Devices (Supersedes IEEE 1532-2000)

For more information on the IEEE Standards:

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For more information on JEDEC:

If your company designs its own ASICs with boundary-scan and you want to get a JEDEC Manufacturer ID Codes (JEP106), please contact JEDEC - Technical Affairs of the Electronic Industries Alliance (EIA) at:

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4 Glossary of Abbreviations:

ASIC	Application Specific Integrated Circuit
AW	AutoWrite
BDM	Background Debug Mode
BGA	Ball-Grid Array
BSDL	Boundary-Scan Description Language
BSR	Boundary-Scan Register
cPLD	Complex Programmable Logic Device
DFT	Design for Test(ability)
DIOS	Digital Input Output Scan
DNP	Do Not Place
DSP	Digital Signal Processor
ECL	Emitter Coupled Logic
FPGA	Field Programmable Gate Array
Hi-Z	High Impedance
I/O	Input - Output
IC	Integrated Circuit
ICT	In-Circuit Test(ing)
IEEE	Institute of Electrical and Electronic Engineers
IP	Intellectual Property
IR	Instruction Register
ISP	In-System Programming
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LSP	Local Scan Port
LVTTTL	Low Voltage Transistor - Transistor Logic
MCGR	Multi-Cast Group Register
OE	Output Enable
PCB	Printed Circuit Board
PLL	Phase Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SI	Scan Input
SO	Scan Output
SRAM	Static Random Access Memory
SSRAM	Synchronous Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TRST	Test Reset
TTL	Transistor - Transistor Logic
UUT	Unit Under Test
VLSI	Very Large Scale Integration
WE	Write Enable

